UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,571	12/20/2001	Eiji Takahashi	NAK1-BQ83	4972

21611 7590 10/22/2003

SNELL & WILMER LLP
1920 MAIN STREET
SUITE 1200
IRVINE, CA 92614-7230

EXAMINER	
TSAI, CAROL S W	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/029,571	Applicant(s) TAKAHASHI ET AL.	
	Examiner Carol S Tsai	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-6 and 30 of Group 1 in Paper No. 8 is acknowledged.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not include the notary's signature, or the notary's signature is in the wrong place.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Publication 2002/0002683 to Benson et al.

Benson et al. disclose a multilayer board (substrate 104 and cover 106 shown on Fig. 2), comprising a signal line requiring tamper-resistance, the signal line including: (a) a conductive trace (conductor paths 134 shown on Fig. 3D) and (b) a conductive via (vias 136 shown on Fig. 3C) that passes through layers of the multilayer board (see paragraphs 0057 and 0071-0072), wherein the conductive trace and an end of the conductive via existing on an outside layer of the multilayer board are placed under one or more circuit components (Electronic components 162 shown on Fig. 6B) mounted on the outside layer (see Fig. 6B; Abstract, lines 1-13; paragraphs 0075-0080 and 0088; page 8, col. 8, claim 1, lines 1-5; and page 9, col. 1, claim 10, lines 1-7).

As to claim 2, Benson et al also disclose a conductive trace (conductor paths 134 shown on Fig. 3D) on an inner layer that is sandwiched between sheets of foil (see paragraphs 0069 and 0070) and/or circuit components (Electronic components 162 shown on Fig. 6B) placed on layers above and below the inner layer (see Fig. 6B) so that the sheets of foil and/or circuit components hide the conductive trace on the inner layer when viewed from above or below (see Figs. 3C and 3D; Abstract, lines 8-13; and paragraphs 0070-0080).

As to claim 3, Benson et al also disclose the sheets of foil placed on the layers that are outside the inner layer are connected to either a ground or a power source (see paragraph 0069).

As to claim 4, Benson et al. also disclose the conductive trace on the outside layer being further covered by a circuit component (Electronic components 162 shown on Fig. 6B) on another outside layer when viewed from above or below (see paragraph 0088).

As to claim 5, Benson et al. also disclose the signal line requiring tamper-resistance being either a signal line that is input to an encryption unit or a signal line that is output from a decryption unit (see paragraph 0024).

As to claim 6, Benson et al. also disclose a multilayer board (substrate 104 and cover 106 shown on Fig. 2), comprising: a certain signal line that includes (a) a conductive trace (conductor paths 134 shown on Fig. 3D) and (b) a conductive via (vias 136 shown on Fig. 3C) that passes through layers of the multilayer board (see paragraphs 0057, 0071, and 0072), wherein the conductive trace and an end of the conductive via existing on an outside layer of the multilayer board are placed under one or more circuit components (Electronic components 162 shown on Fig. 6B) mounted on the outside layer (see Fig. 6B; Abstract, lines 1-13; paragraphs 0075-0080 and 0088; page 8, col. 8, claim 1, lines 1-5; and page 9, col. 1, claim 10, lines 1-7), the certain signal line further includes a conductive trace (conductor paths 134 shown on Fig. 3D) on an inner layer that is sandwiched between sheets of foil (see paragraph 0069) and/or circuit components (Electronic components 162 shown on Fig. 6B) placed on layers above and below the inner layer (see Fig. 6B) so that the sheets of foil and/or circuit components hide the conductive trace on the inner layer when viewed from above or below (see Figs. 3C and 3D; Abstract, lines 8-13; and paragraphs 0070-0080), and the certain signal line is either a data line or an address line (paragraph 0007).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No. 5,956,415 to McCalley et al.

McCalley et al. disclose a tamper-resistant multilayer board for transfer of pixel data to be encrypted (see col. 3, lines 1-11 and lines 53-67; col. 7, lines 31-42; and col. 10, lines 45-59) comprising: a board member (a secure sensor package 190 shown on Fig. 22), having a plurality of layers and one or more components mounted thereon (see Figs. 7 and 22 and col. 6, lines 32-63); a reception/decryption unit mounted on the board member (see col. 3, lines 43-52 and col. 11, lines 6-10); and output interface unit (encrypted output circuit 194 shown on Fig. 22) mounted on the board member (a secure sensor package 190 shown on Fig. 22) and operatively connected to the reception/decryption unit (see col. 3, lines 43-52 and col. 11, lines 6-10); and a conductive path (see col. 5, lines 50-61; col. 6, lines 33-63; and col. 11, lines 6-15) operatively designed for interconnecting the reception/decryption unit and output interface unit and position adjacent an interior layer surface for a portion of the conductive path and positioned under one or more components (processor 192 and destructible memory 193 shown on Fig. 22) for the remainder of the conductive path to prevent direct access from the exterior of the board member (see Figs. 7 and 22 and col. 10, line 45 to col. 11, line 23).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gailus discloses a multi-layer printed circuit board including a non-conductive via which intersects a conductive trace on an inner layer of the board and is adapted to receive a conductive element configured to make direct contact with the conductive trace.

Kommerling discloses an integrated circuit device comprising: a circuit which uses

encryption; and an encapsulation packaging layer; in which the circuit is responsive to at least one physical parameter of the encapsulation to apply the encryption and/or decryption by reading the key therefrom, so that tampering with the encapsulation to gain access to the circuit causes the encryption and/or decryption to fail.

Goetz et al. disclose a system and method for efficiently interconnecting a plurality of ICs, thereby improving the electrical performance of the overall system while reducing contact degradation due to stress that results from differences in the coefficients of thermal expansion of the various components during thermal cycling.

Chung discloses a wireless article, such as an identification tag or badge, including an electronic device mounted on a substrate and connected a loop antenna for receiving and/or transmitting radio frequency signals.

Kocher et al. disclose a secure cryptographic rights unit for cryptographically regulating access to digital content includes an interface control processor and a specialized cryptographic unit that protects access to a memory.

Ciacelli et al. disclose apparatus, method and computer program product being provided for digitally processing an encrypted data stream scrambled, for example, according to content scrambling system (CSS) technology.

Novak et al. disclose a system and method being presented for stabilizing the electrical impedance of a structure (e.g., an electrical interconnecting apparatus) including a pair of parallel planar conductors separated by a dielectric layer.

Saccocio discloses a multi-layer printed-wiring board the ground and power conductor-

bearing layers being placed immediately (without intermediancy of other conductive layers) below the outer surface conductor-bearing layers and being connected to the outer surface layers by micro-vias that do not extend beyond the ground and power layers, whereby the micro-vias avoid causing trace-routing blockages on lower, signal-routing, layers.

Curiel discloses methods of creating tamper resistant informational articles and related products.

Van de Steeg et al. disclose a structural key being checked under program control to control the mode of operation for a processor-based electronic circuit board.

Byrne discloses a tamper resistant structure having a pattern which covers portions of an IC but exposes other portions of the IC so that etching away the tamper resistant structure destroys the exposed portions.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. Tsai whose telephone number is (703) 305-0851. The examiner can normally be reached on Monday-Friday from 7:30 AM to 4:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703) 308-1677. The fax number for TC 2800 is (703) 308-7382. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (703) 308-1782.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 308-7382. This practice

may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Patent Examiner
Art Unit 2857

10/13/03